Common Source JFET Amplifier Experiment

Mindy Hull
11/1/24

Objectives: The objectives of this laboratory exercise are to: 1) model a JFET common source amplifier circuit using SPICE simulation software, 2) prototype the circuit and compare testing results to the simulation, and 3) validate manual mathematical circuit analysis results.

SPICE Simulation Software:
NI Multisim 14.3, student version

Prototype Equipment:
Components
- JFET (2N5457, ON Semiconductor)
- Capacitors
  - (one) 0.01µF
  - (one) 1µF
  - (one) 10µF
- Resistors (nominal/measured)
  - (one) 1MΩ / 0.95MΩ
  - (one) 3kΩ / 3.257kΩ
  - (one) 10kΩ / 9.85kΩ
  - 1kΩ potentiometer (maximum measured resistance = 1.04kΩ, minimum measured resistance = 1.63Ω)

Test Equipment:
- Topward 8112 Digital Function Generator
- Fluke 45 Multimeter
- Tektronix 2465 300MHz Oscilloscope
- Kaito HY3003D-3 Linear Voltage Supply

Breadboard, jumper wires

References:
Andrew Bell. Making a JFET model in Multisim *[video]*. YouTube. November 20, 2019 https://www.youtube.com/watch?v=mB1n_yOS2Qc&t=46s

Floyd TL. Electronic devices: conventional current version, 10th edition, global edition. Pearson Education Limited, 2018.

Electronics With Professor Fiore. Semiconductor devices: JFET common source amplifier *[video]*. YouTube. April 24, 2020 https://www.youtube.com/watch?v=2Pu5wZnRxRo

On Semiconductor, "JFETs – general purpose N-channel – depletion" 2N5457, 2N5458 datasheet, Feb 2010, rev 6.

CIRCUIT UNDER TEST SPICE SOFTWARE SIMULATION:

Methods: The common source JFET experimental circuit under test (*Figure 1, Figure 2*) was constructed using NI Multisim 14.3 SPICE simulation software. This circuit is based on a reference circuit that was provided elsewhere. For this experiment two circuits were built, in particular one where the source resistor, labeled "R3" on circuit diagrams, was assigned a value of 1.63Ω and another where

the source resistor was assigned a value of 1kΩ. In the original reference circuit, the source resistor is a 1kΩ potentiometer. Therefore in this simulation, these source resistor values were selected in order to simulate the measured high end of the potentiometer resistance (i.e.,1kΩ) as well as the low end of the potentiometer resistance (1.63Ω). These resistors are labeled “POT high” and “POT low” on the circuit diagrams to reflect this.

Within Multisim, the ability to select a two-channel oscilloscope analytical module exists. One channel of the oscilloscope measured a probe placed between the positive node of the AC 100mVp 1kHz signal source and ground. The other probe was placed on either side of the load resistor (labeled R4 on circuit diagrams). The load resistor was in series with a 1µF capacitor (labeled C_2), which directly attached to the drain terminal of the JFET.

Additionally, a multimeter probe is placed on either side of the load resistor, and measures AC RMS output voltage.

The JFET itself needed to be modeled using a Multisim tool called “Component Wizard” under the “Tools” tab. Andrew Bell’s video (see references) is particularly helpful in constructing the 2N5457 JFET specifically. The model data that needs to be inputted into the software is:

.MODEL 2N5457A NJF(IS=1N VTO=-1.5 BETA=1.125M LAMBDA=2.3M CGD=4PF CGS=5PF)

Results: Multisim simulations showing oscilloscope and multimeter results for the circuit under test are shown.

Figure 1. JFET amplifier with relatively high source resistance.

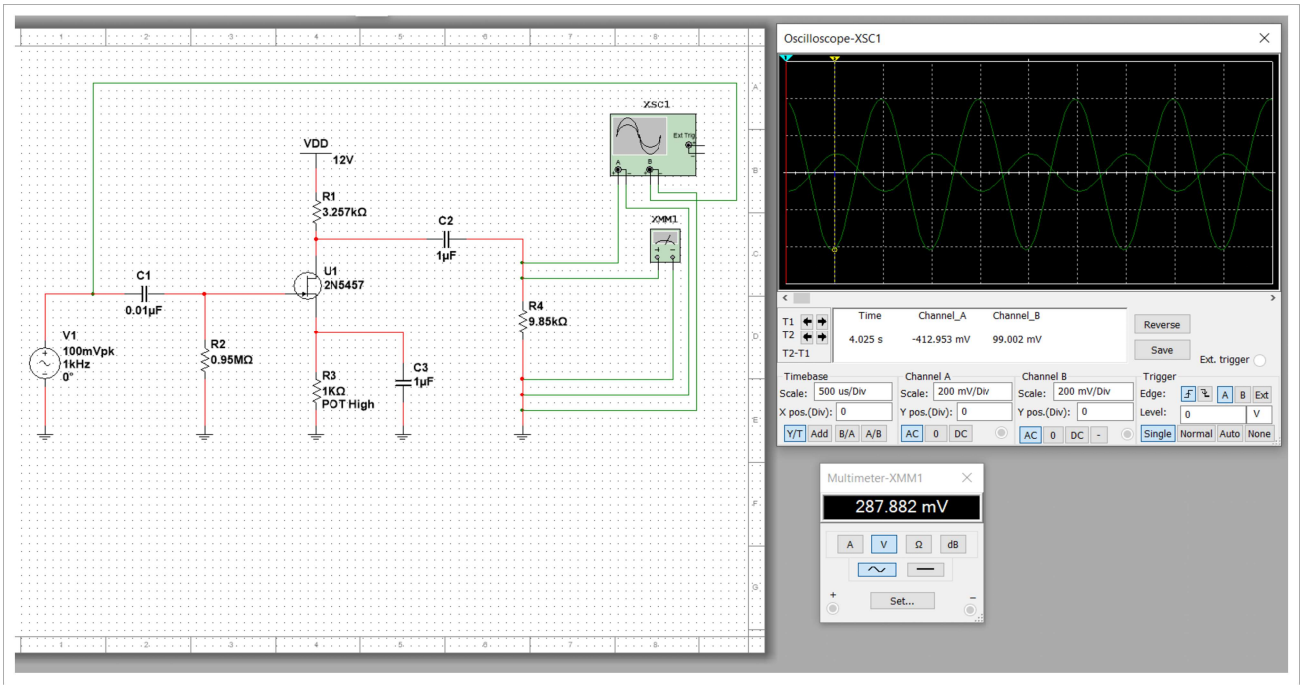


Figure 1 shows the circuit under test on the left with R3 (i.e., the source resistor) approximating the high end of the potentiometer (i.e., 1kΩ) resistance. Channel B of the oscilloscope confirms an input

sinusoidal peak voltage around 100mV. Channel B shows the results of the JFET amplification across the load resistor (R4), with an output of 413mV$_P$AC. The output signal is 180 degrees out of phase with the input signal. The multimeter graphic also shows an AC voltage across R4 of 287.9mV$_{RMS}$ which corresponds to 405.8mV$_P$.

Figure 2. JFET amplifier with relatively low source resistance.

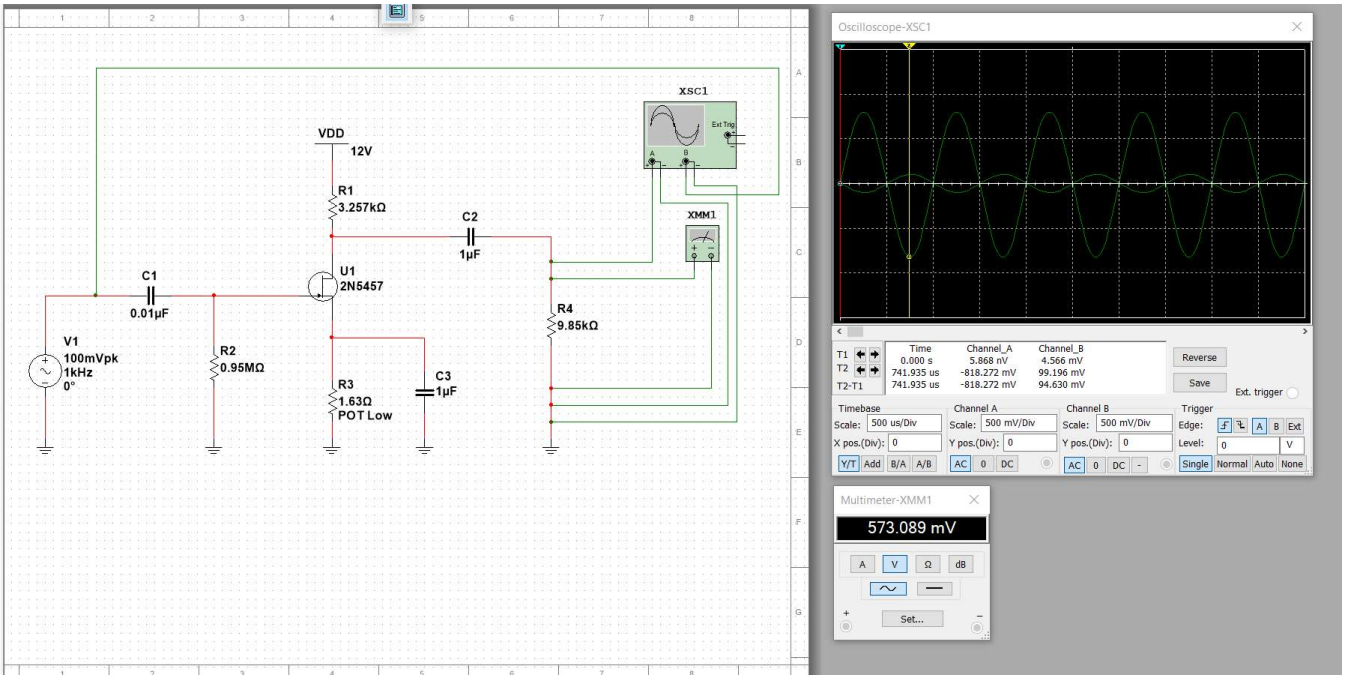


Figure 2 demonstrates the JFET amplifier with a negligible source resistance of 1.63Ω. Again the oscilloscope channel B confirms that the AC signal source is around the assigned 100mVp. The output signal across the load resistor (R4) is again 180 degrees out of phase with the input signal. The output signal is also 8.7 times larger than the input signal, registering 818.3mV$_P$AC on channel A of the oscilloscope. The simulation of this circuit under test demonstrates that a lower R_S creates a higher voltage across the load resistor.

CIRCUIT UNDER TEST PROTOTYPE

Methods: The circuit under test was constructed on a prototyping breadboard using discreet through-hole components (*figure 3*). A function generator inputted an AC sinusoidal 100mVp / 1kHz signal into the gate terminal of the JFET, while VDD was 12VDC into the drain terminal from a linear power supply. Testing of the circuit was analogous to that used in the SPICE simulation, including an oscilloscope probe across the output of the signal source (R4) and the reference ground, and an oscilloscope probe across the load resistor. A digital multimeter was used to determine actual values of resistors used to construct this circuit, and these actual measured values were used in the SPICE simulation rather than nominal values.

Results: The sinusoidal input signal is shown in Figure 4, and is 200mV$_{PP}$AC, which of course corresponds to a peak voltage of 100mVAC.

Figure 3. Circuit under test breadboard configuration.

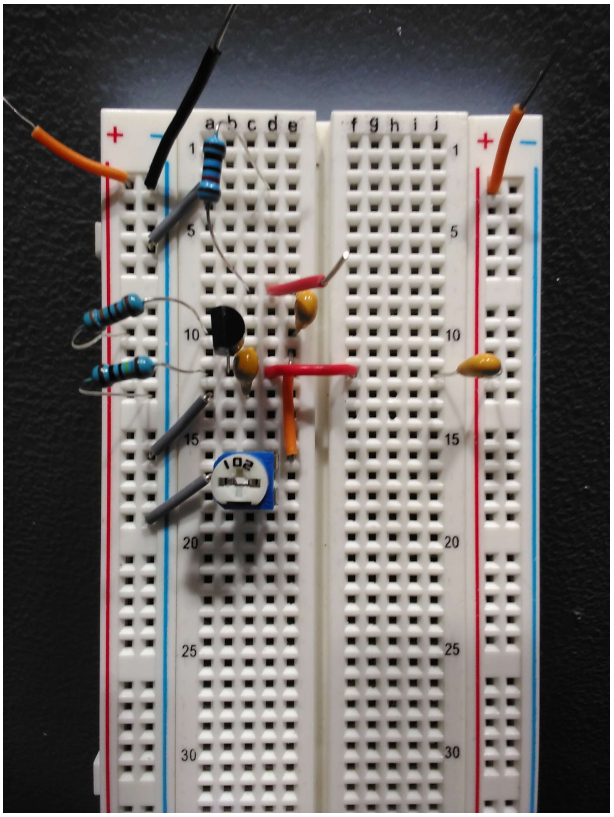


Figure 4. Sinusoidal input signal showing 200mV$_{PP}$ AC voltage.

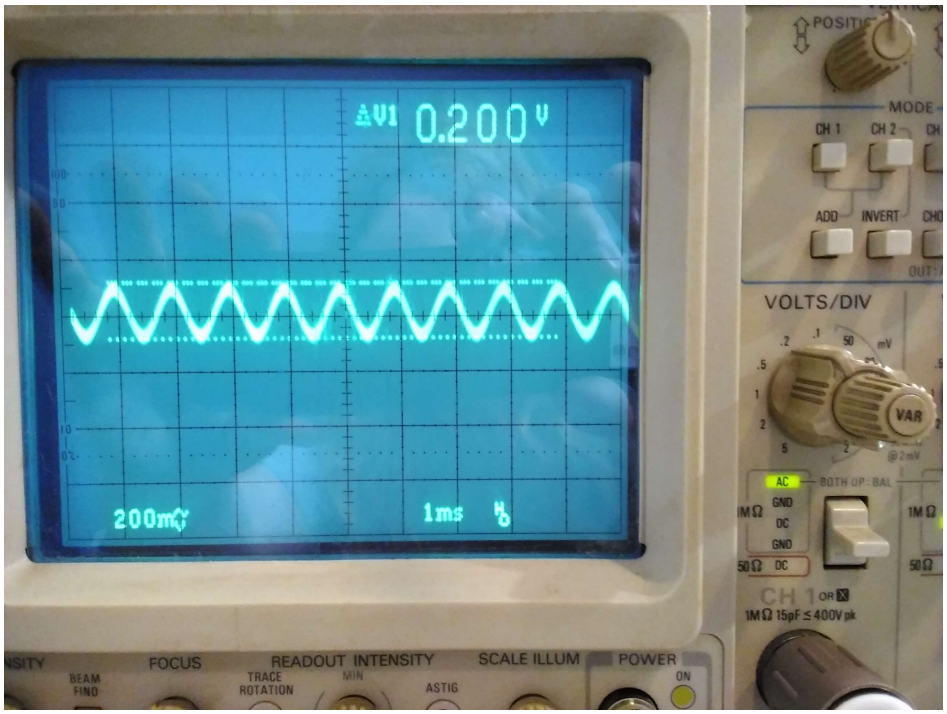


Figure 5 shows the oscilloscope trace across the load resistor (R4) when the source resistance (R3) potentiometer is set to its maximum resistance of nominally 1kΩ (measured 1.04kΩ). The AC sinusoidal output signal is 725mV peak-to-peak, which corresponds to a 362.5mV peak voltage, or 256mV RMS. Figure 6 shows the input signal (bottom) contrasted with the output signal (top). Note that the oscilloscope is set to 200mV/div in all of these traces. The output signal is 180° out of phase with the input signal. In comparison, the SPICE simulation shows an output signal voltage (413mV$_P$AC) that is 13.9% higher than the prototyped circuit when the source resistance is 1kΩ.

*Figure 5. Output signal of 725mV$_{PP}$AC (362.5mV$_P$AC) when the source resistance is 1k*Ω.

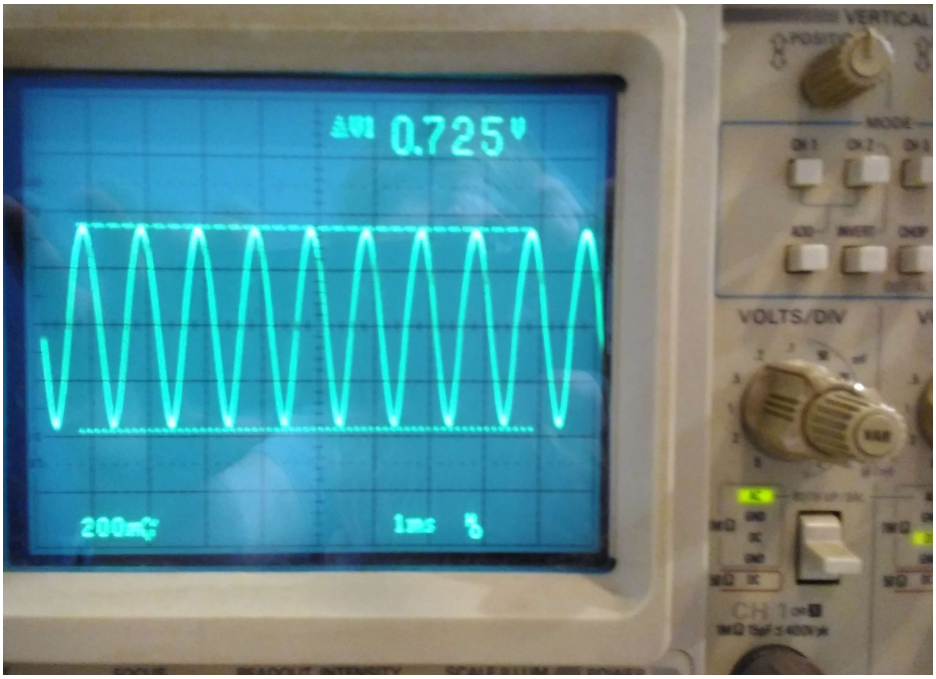


*Figure 6. Output signal (top) compared to input signal (bottom) with max. source resistance of 1k*Ω.

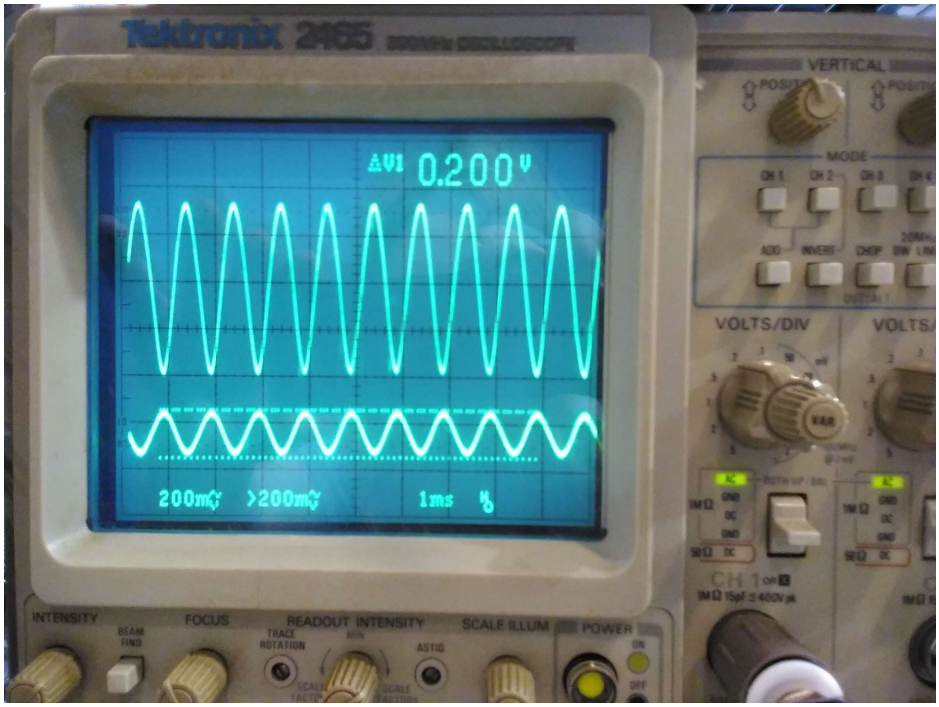


Figure 7 shows the oscilloscope trace across the load resistor (R4) when the source resistance (R3) potentiometer is set to its minimum resistance of nominally 0Ω (measured 1.63Ω). The AC sinusoidal output signal is 1280mV peak-to-peak, which corresponds to a 640mV peak voltage, or 452.5mV RMS. Figure 8 shows the input signal (bottom) contrasted with the output signal (top). The output signal is 180° out of phase with the input signal. In comparison, the SPICE simulation shows an output signal voltage (818.3mV$_P$AC) that is 27.9% higher than the prototyped circuit when the source resistance is 1.63Ω.

Figure 7. Output signal of 1280mV$_{PP}$AC (640mV$_P$AC) when the source resistance is 1.63Ω.

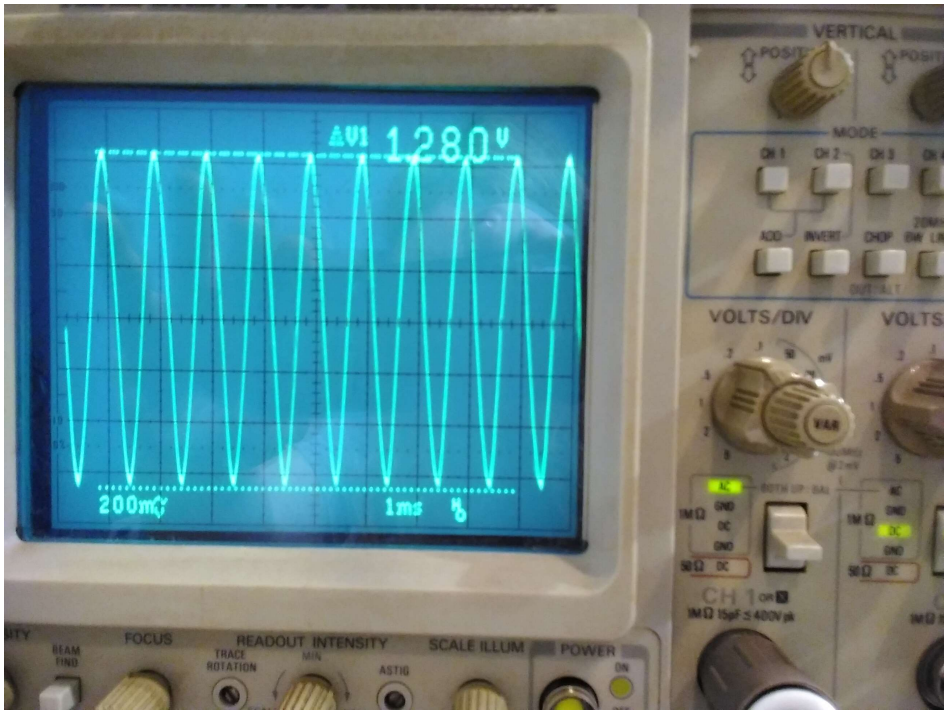
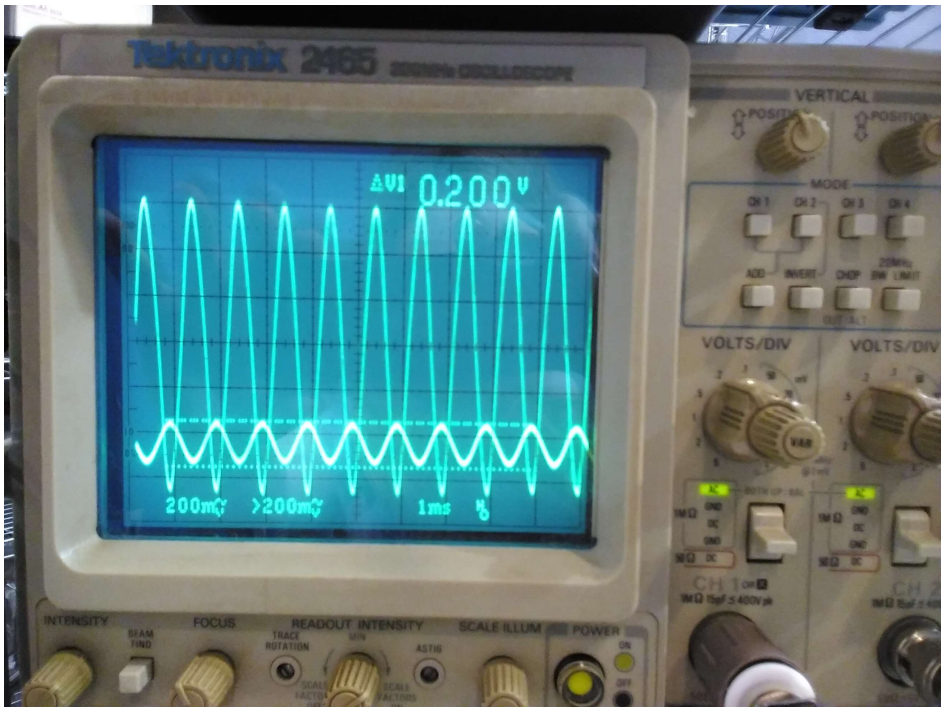


Figure 8. Output signal (top) compared to input signal (bottom) with min. source resistance of 1.63Ω.



MATHEMATICAL CIRCUIT ANALYSIS

Methods: The JFET common-source amplifier circuit under test is analyzed mathematically to determine the loaded voltage gain. This is done first by analyzing a DC equivalent circuit to determine drain current (I_D) and gate-source voltage (V_{GS}). The 2N5457 JFET has an I_{DSS} of 5mA and a $V_{GS(OFF)}$ of -3.5V according to its published datasheet (see references). I_D is determined from the published common source transfer characteristics graph (also available in the datasheet). Analysis of the AC equivalent circuit is utilized to determine the voltage gain (A_V) of the circuit for both the source resistance of 1.04kΩ and 1.63Ω.

Results: The common source transfer characteristics curve from the ON Semiconductor datasheet for the 2N5457 JFET is used to determine the I_D and V_{GS} for the source resistance R_s (i.e., R_3 on circuit diagram). A load line is determined by connecting the origin to the point (V_{GS}, I_{DSS}).

For R_S = 1.04kΩ:

$V_{GS} = -I_{DSS} * R_S = -5mA * 1.04k\Omega = -5.2V$

At the Q-point (intersection), the I_D = 1.5mA, and the V_{GS} = -1.6V

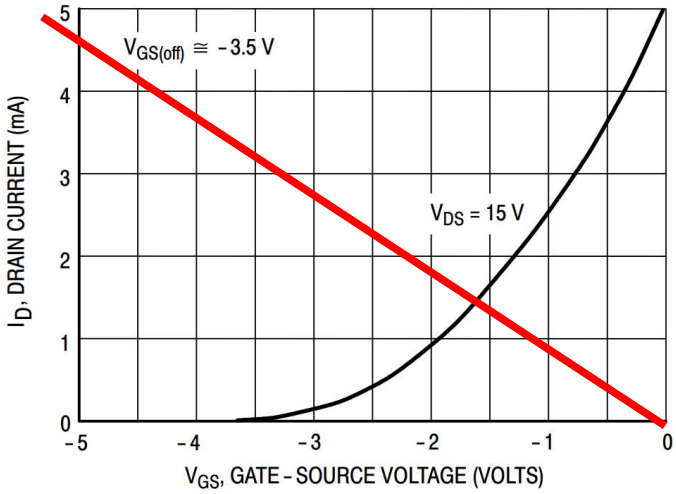


Figure 5. Common Source Transfer Characteristics

$V_D = V_{DD} – I_D R_D = 12V – (1.5mA * 3k\Omega) = 7.5V$

$g_{m0} = 2\ I_{DSS} / |\ V_{GS(OFF)}\ | = (2 * 5mA) / 3.5V = 2.86mS$

$g_m = g_{m0} [1 – (\ V_{GS} / V_{GS(OFF)}\ ) = 2.86mS [1 - (-1.6V / -3.5V) = 1.55mS$

$V_{OUT} = A_V V_{in} = g_m R_D V_{IN} = 1.55mS * 3k\Omega * 100mV = 465mV$

Mathematical calculations show that for a source resistance of 1.04kΩ, the circuit under test has an unloaded signal output of 465mV_PAC.

With a 10kΩ load resistor:

$R_d = R_D R_L / R_D + R_L = (3k\Omega * 10k\Omega) / (3k\Omega + 10k\Omega) = 2.31k\Omega$

$V_{OUT} = A_V V_{in} = g_m R_d V_{IN} = 1.55mS * 2.31k\Omega * 100mV = 358mV$

Mathematical calculations show that for a source resistance of 1.04kΩ, the circuit under test has a signal output of $358mV_PAC$ when loaded with a 10kΩ resistor. This calculated result is remarkably close to the prototype result which had a measured signal output of $362.5mV_PAC$.

For $R_S = 1.63\Omega$:

$V_{GS} = -I_{DSS} * R_S = -5mA * 1.63\Omega = -8.15mV$

At the Q-point (intersection), the $I_D = 5mA$, and the $V_{GS} = -0.1V$

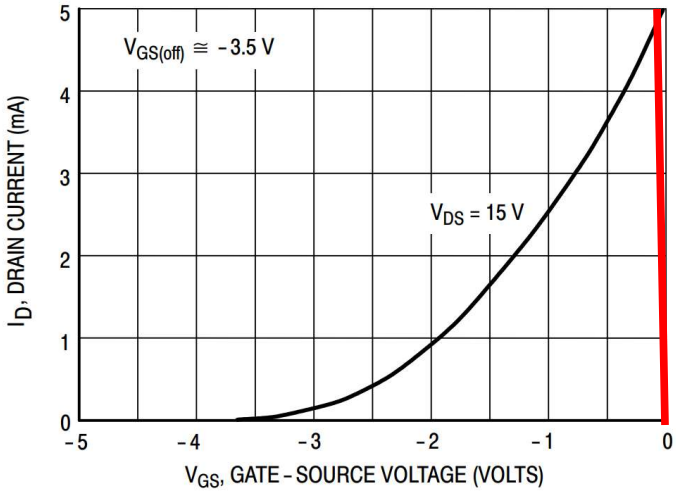


Figure 5. Common Source Transfer Characteristics

$V_D = V_{DD} – I_D R_D = 12V – (5mA * 3k\Omega) = -3V$

$g_{m0} = 2 I_{DSS} / | V_{GS(OFF)} | = (2 * 5mA) / 3.5V = 2.86mS$

$g_m = g_{m0} [1 – (V_{GS} / V_{GS(OFF)}) = 2.86mS [1 - (-0.1V / -3.5V) = 2.77mS$

$V_{OUT} = A_V V_{in} = g_m R_D V_{IN} = 2.77mS * 3k\Omega * 100mV = 833mV$

Mathematical calculations show that for a source resistance of 1.63Ω, the circuit under test has an unloaded signal output of $833mV_PAC$.

With a 10kΩ load resistor:
$R_d = R_D R_L / R_D + R_L = (3k\Omega * 10k\Omega) / (3k\Omega + 10k\Omega) = 2.31k\Omega$

$V_{OUT} = A_V V_{in} = g_m R_d V_{IN} = 2.77mS * 2.31k\Omega * 100mV = 639mV$

Mathematical calculations show that for a source resistance of 1.63Ω, the circuit under test has a signal output of 639mV$_P$AC when loaded with a 10kΩ resistor. This calculated result is nearly identical to the prototype result which had a measured signal output of 640mV$_P$AC.

DISCUSSION

This laboratory analyzed a JFET common source amplifier circuit under test using three different methods: SPICE simulation, prototyping with discreet components, and mathematical calculation. Source resistance was chosen as an independent variable, with voltage across the load resistance as the dependent variable. As source resistance decreased from 1kΩ to nearly 0Ω, the inverted output signal voltage increased in amplitude.

Analysis of the circuit under test with mathematical calculation and prototyping showed remarkably similar results. With a standardized sinusoidal gate input signal of 100mV$_P$AC, and a source resistance of 1kΩ, the output signal was measured to have a voltage of 362.5mV$_P$AC, for an $A_V = V_{OUT} / V_{IN} =$ 3.625. The computed output was 358mV$_P$AC. On the other hand, the SPICE simulation output was 413mV$_P$AC. This discrepancy may be due to how the JFET was modeled, and a topic which is beyond the scope of this laboratory exercise.

Similarly, with the same 100mV$_P$AC input signal, but with the source resistance decreased to 1.63Ω, the output signal of the prototype, mathematical, and simulated circuit models was 640mV$_P$AC, 639mV$_P$AC, and 818.3mV$_P$AC, respectively. Again, the SPICE simulation seems the least accurate, which has probably more to do with the user than the actual software. The gain seen by the prototyped circuit under test was $A_V = V_{OUT} / V_{IN} = 6.4$.

CONCLUSION

A self-biasing common source JFET amplifier circuit can use variations in source resistance to vary the signal output, with lower source resistance producing a greater output signal gain. Further work is necessary to understand why the SPICE simulation is not congruent with the directly measured prototype and computational models of this circuit.
